High Speed Design Basics

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Agenda

1. What is a High Speed PCB?
2. Stackup and Floorplanning
3. Impedance and Routing

What is a High Speed PCB?

What is a High Speed PCB?

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- A circuit board that transmits/receives a lot of digital data
- Tends to have high data rate (Mbps and higher)
- Common computing peripherals (USB, DDR, PCIe…)
- Common vision/AV peripherals (MIPI, HDMI, LVDS…)
- ***The clock rate does not determine if a component operates at high speed***

- ***How to be successful at your first high speed design:***
- Understand stackup design
- Understand differential pairs and how to route them
- Understand return paths and what causes EMI
- Understand high speed signaling standards (USB, DDR, PCIe…)
- Understand power integrity → ***Power is not DC!***

Digital Data Formats

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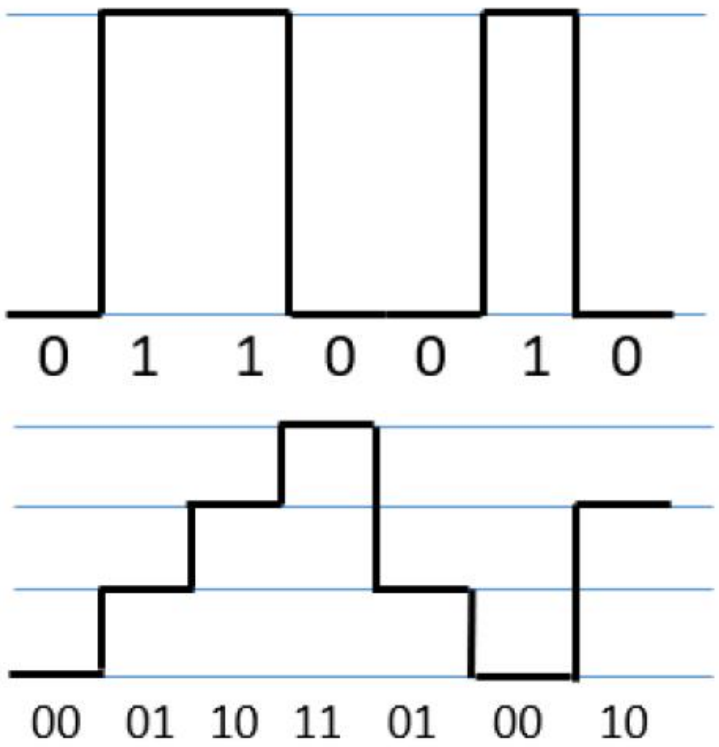
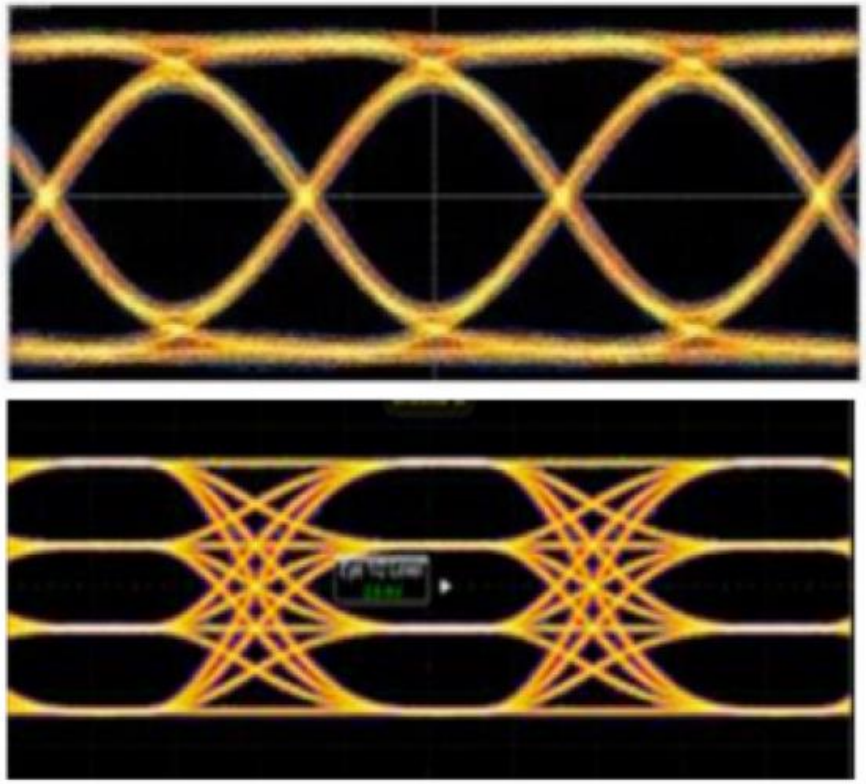
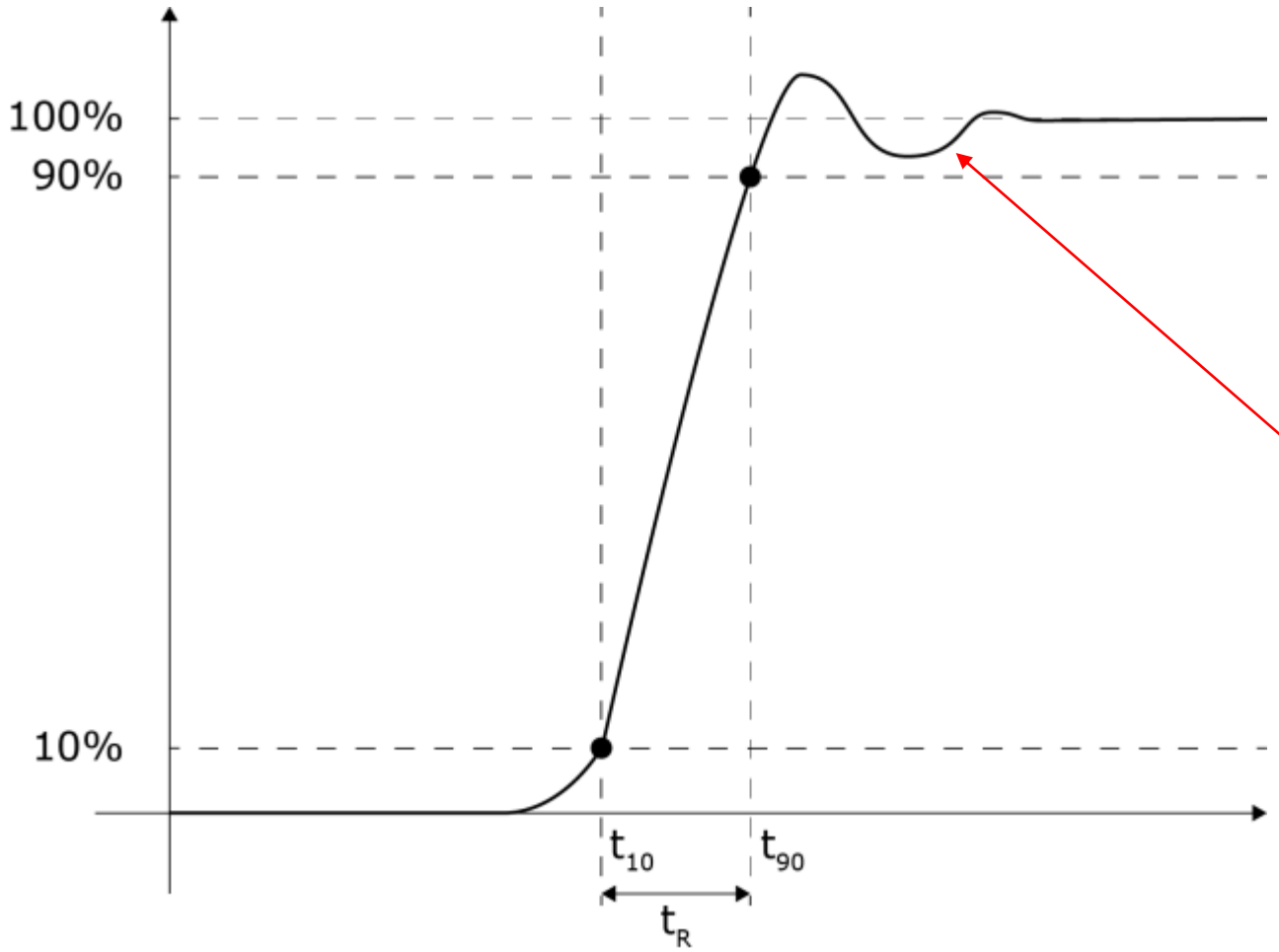
- Single-ended (e.g., SPI)
- Differential
- Differential + multi-level (e.g., PAM4 in PCIe 6.0)





Digital Signals and Rise Time

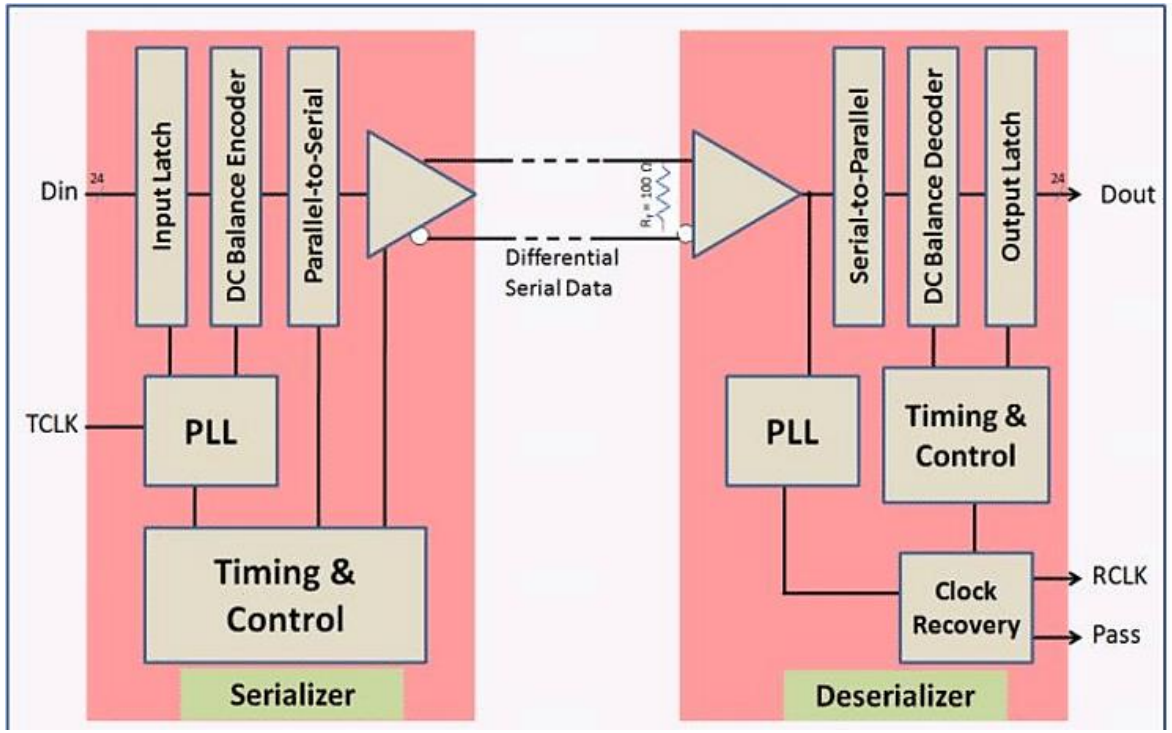
- Signal rise time ($\frac{dI}{dt}$ and $\frac{dV}{dt}$) governs electrical behavior



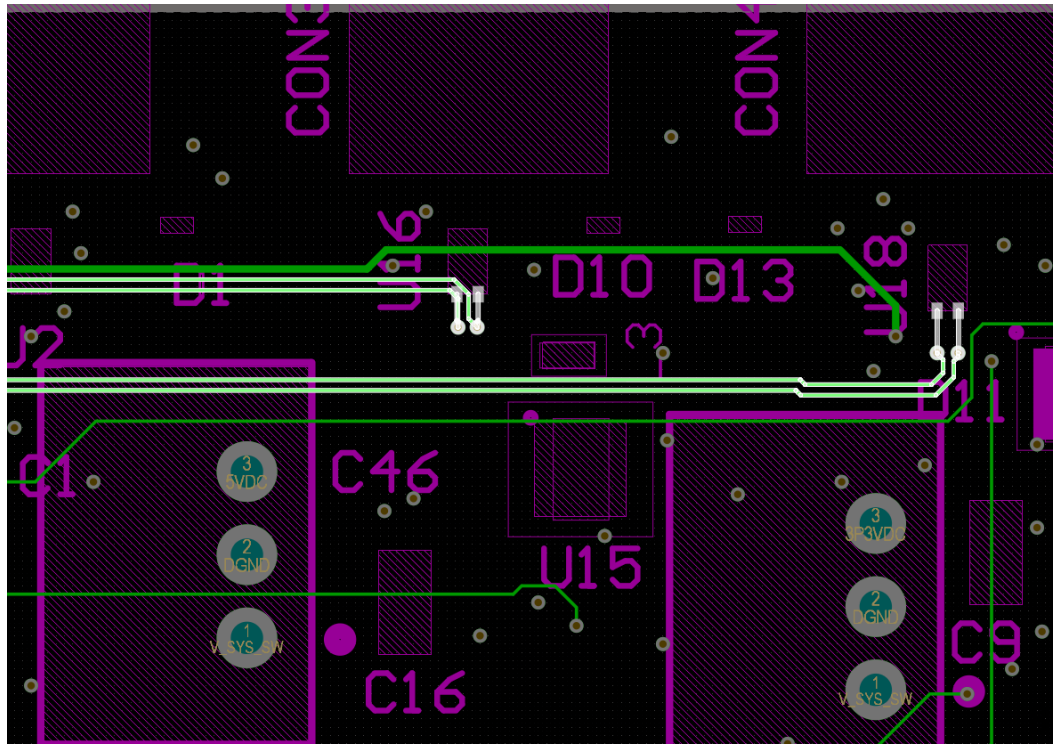
- Crosstalk
- Radiated emissions
- Measurement artifacts (Gibbs)
- Transient phenomena
- Resonant phenomena

Digital Protocols – SerDes

- Most modern high-speed digital is differential
- Around 2005, shift away from parallel buses to serial in PCs

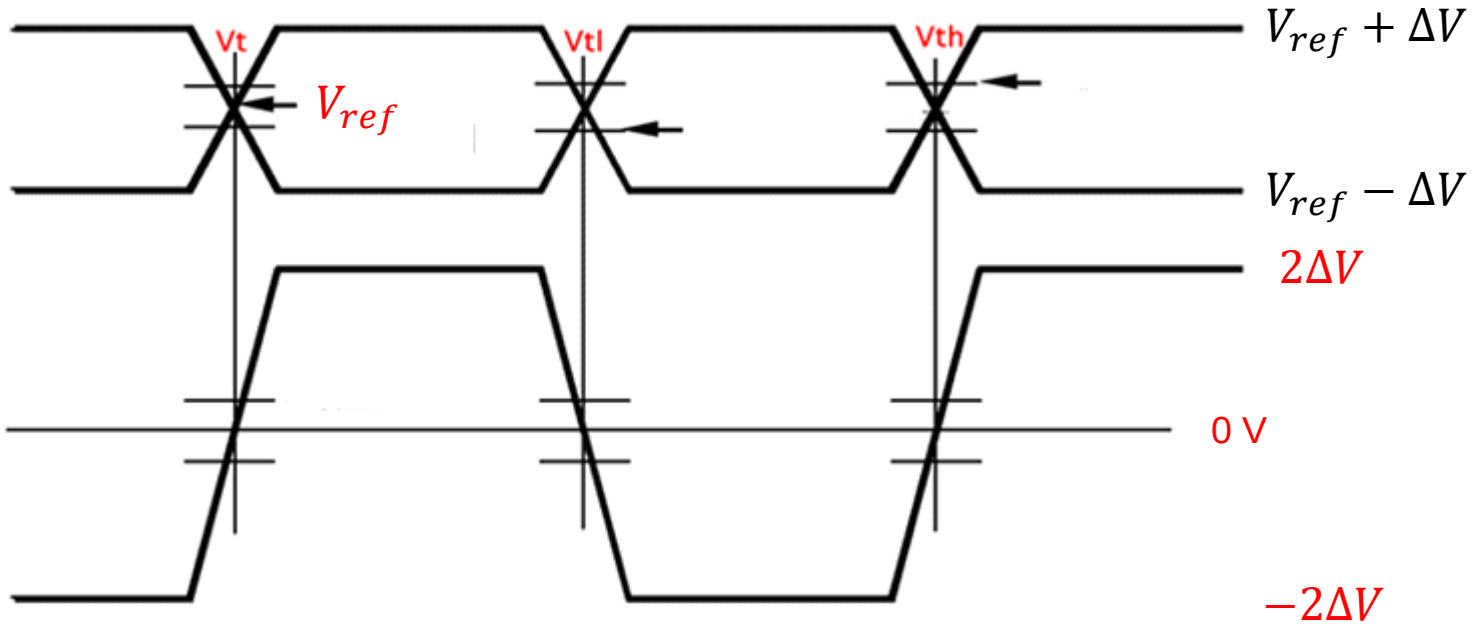


On a PCB: Two traces routed together



Digital Protocols – Differential Pairs

- Equal and opposite polarity signals, may have some DC offset

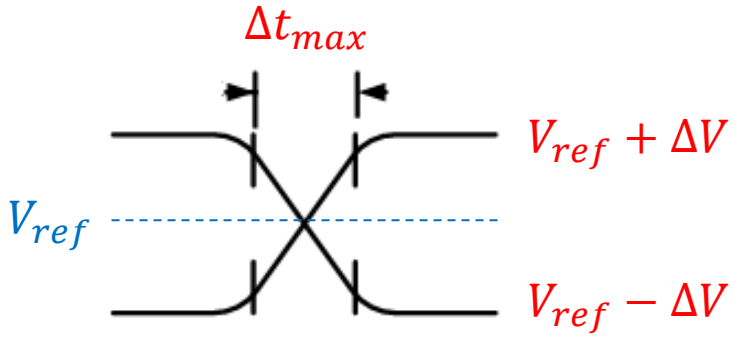


- Main noise benefit: can withstand some crosstalk/common-mode noise:

$$V_{\pm} = \pm[(V_{ref} + \Delta V + V_N) - (V_{ref} - \Delta V + V_N)]$$
$$= \pm[\Delta V - (-\Delta V)]$$
$$\boxed{= \pm 2\Delta V}$$

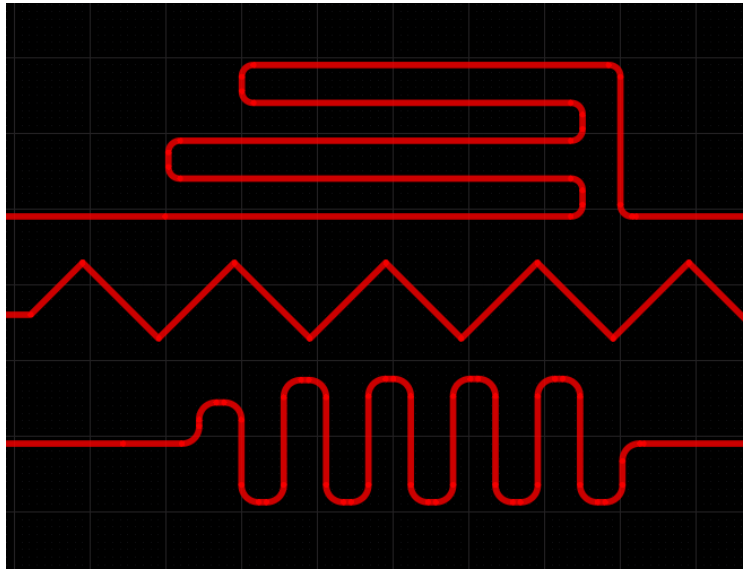
Differential Receivers

- Receivers detect crossing signal swings:



- Maximum length mismatch:

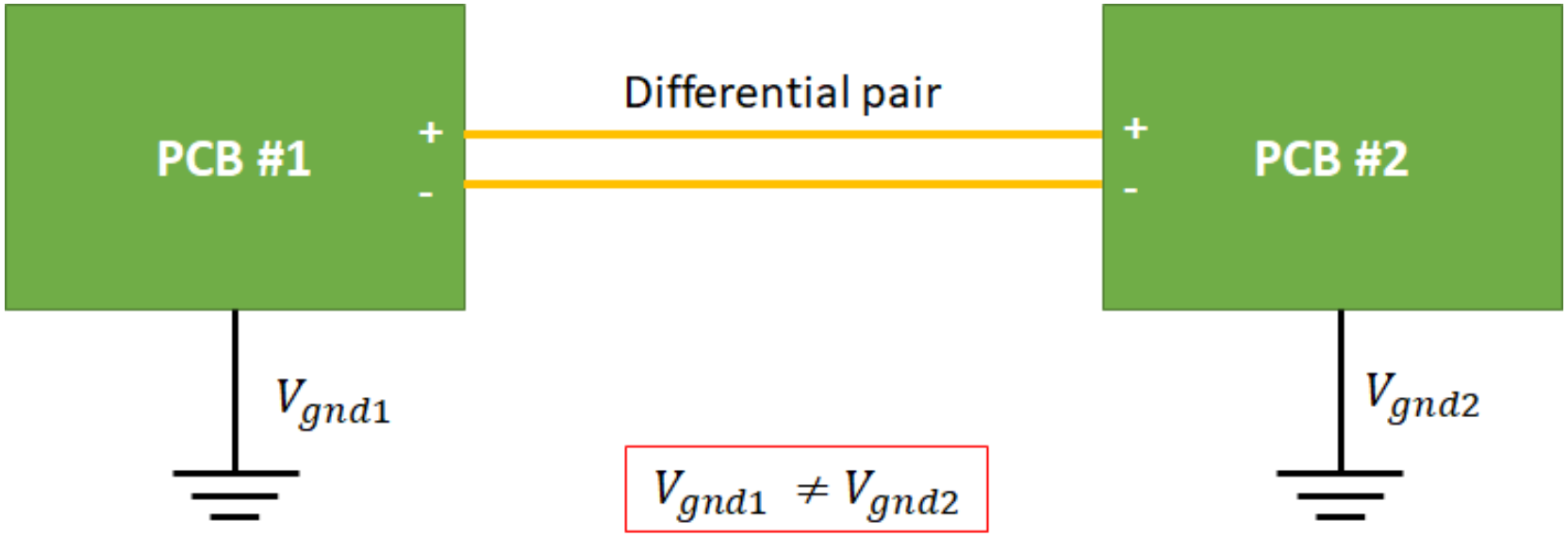
$$\Delta L_{max} = v \Delta t_{max}$$



Why Differential Pairs Are Used?

- Signals emit differential-mode radiated noise → less crosstalk and radiated noise

- Withstand large ground offsets between boards



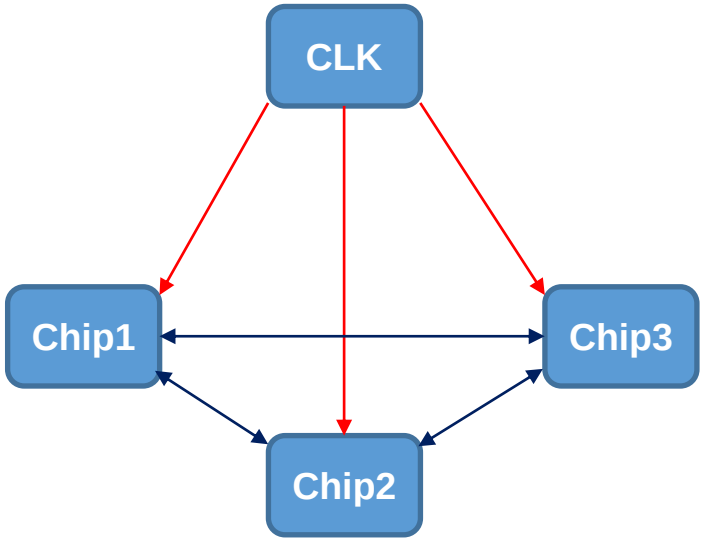
- On each PCB → Ground still needed for signal integrity

Digital Protocols – Serial Data + Embedded Clock

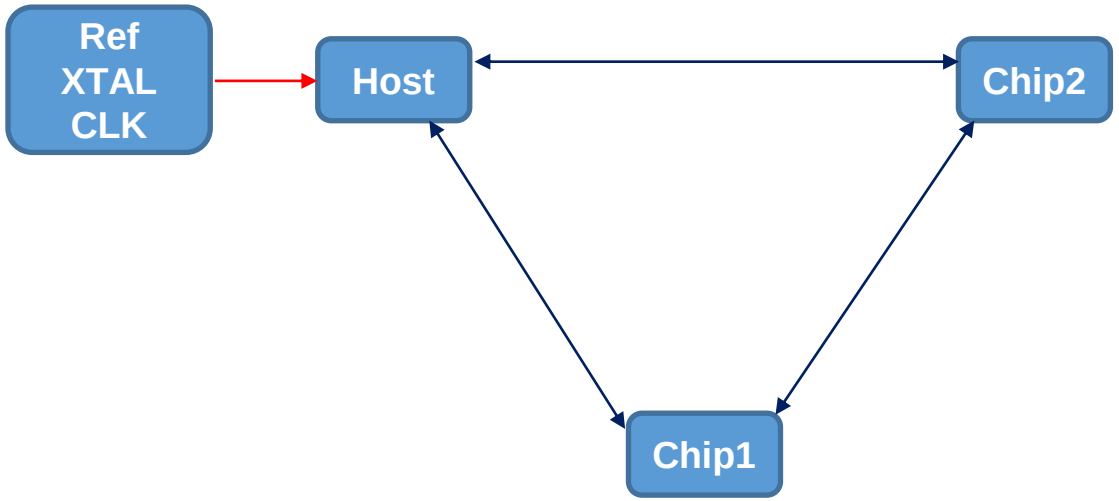
- Most protocols use an embedded clock (DDR uses dedicated differential pair)

- 2-wires = easier routing with very high data rates

Low-speed, RF: **System or source-synchronous clock**



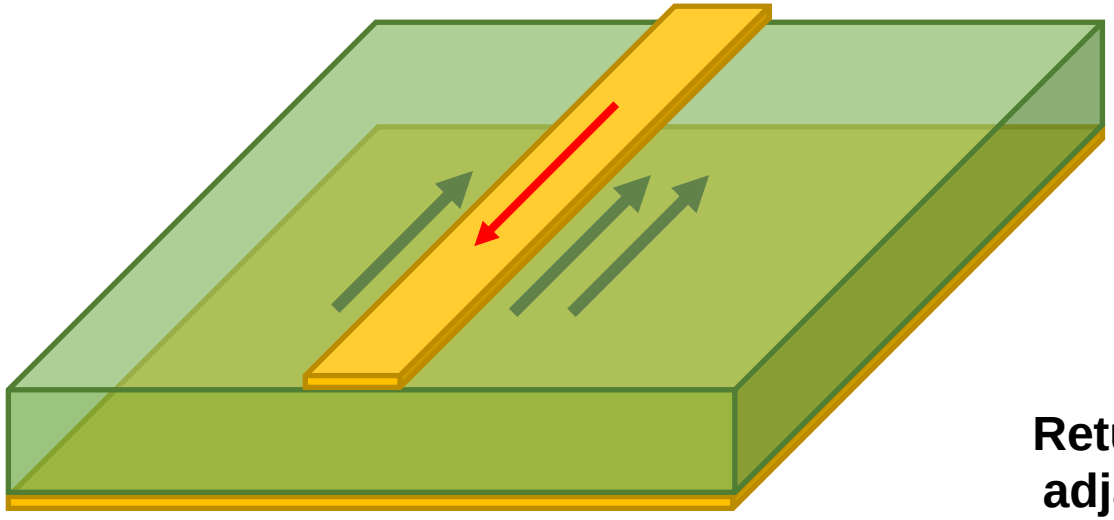
High-speed: **Embedded clock**

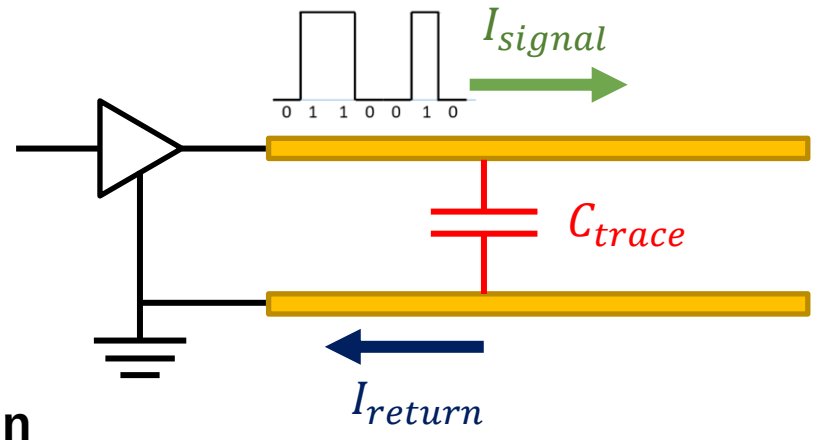


Stackup and Floorplanning

- Most noise problems created or solved in the PCB stackup

- Stackup determines the return path location → signals need close ground





Return current in adjacent copper

- ***<u>High speed PCBs need ground planes</u>***

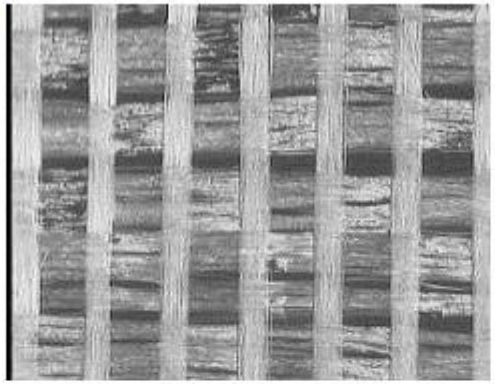
- ***Shopping list for stackups***
- SI properties: weave tightness, Dk/Df values
- Mechanical/thermal properties: Tg value, thermal conductivity, CTE
- Copper weight: Usually 1 oz./sq. ft. or 0.5 oz./sq. ft.
- Layer thickness
- Prepreg vs. core order

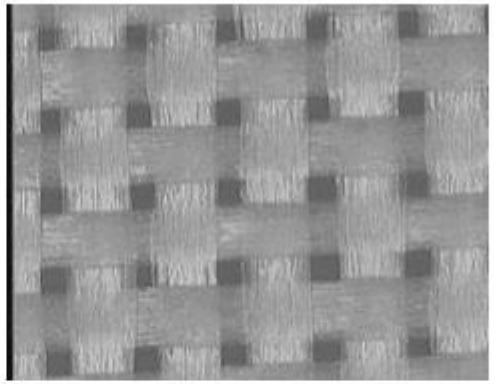
Glass Weave Styles

- Numeric code used to denote glass weave styles
- Laminate providers can give more information and options

FR4 Pre-preg **106**

Thickness 50 µm
Resin content ~70%



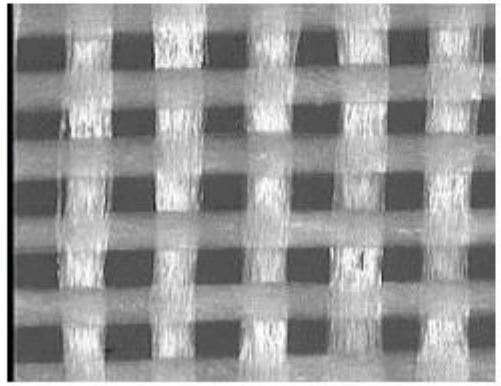


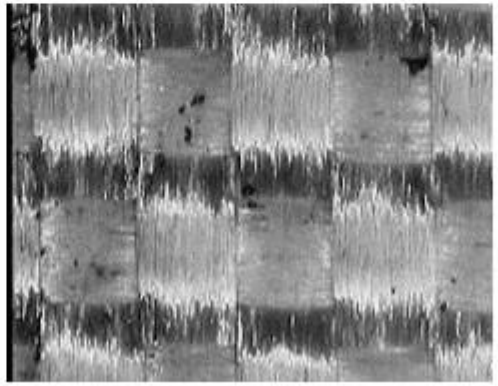
FR4 Pre-preg **2116**

Thickness 90 – 110 µm
Resin content ~50%

FR4 Pre-preg **1080**

Thickness 60 - 70 µm
Resin content ~60%





FR4 Pre-preg **7628**

Thickness 170 – 190 µm
Resin content ~45%

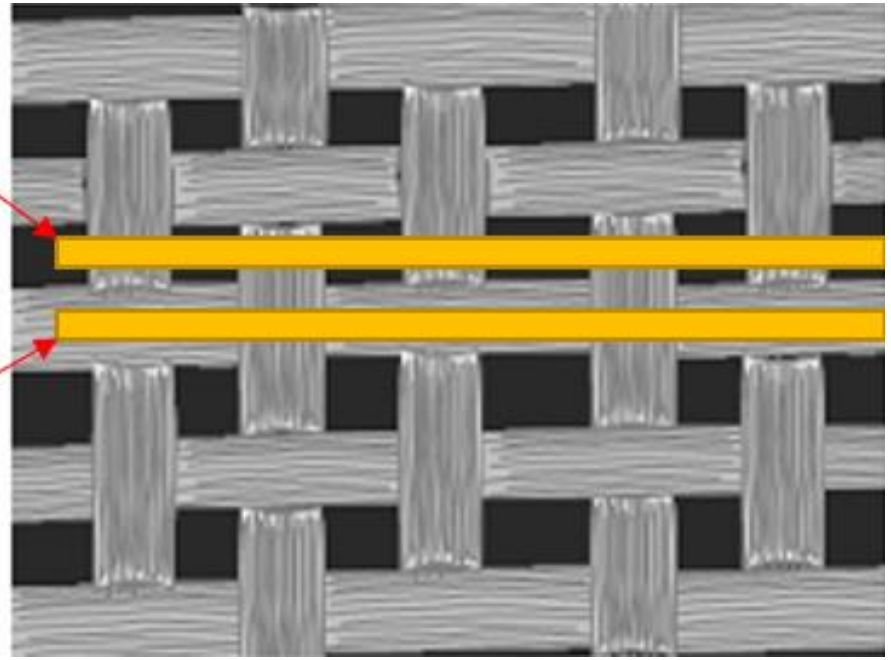
Glass Weave Styles

- Glass weave style creates skew in differential pairs

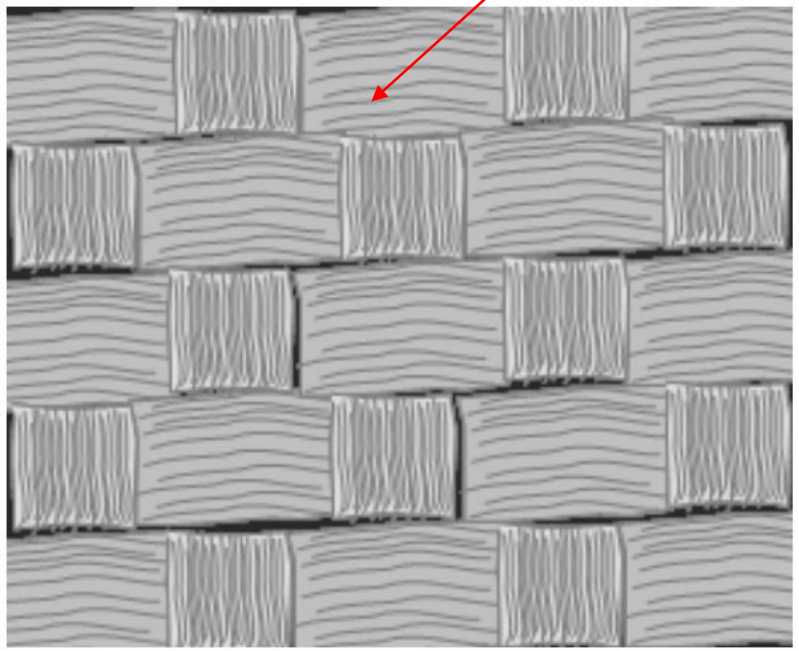
$$\varepsilon_{resin} < \varepsilon_{fiber}$$

Skew accumulates in this trace

No skew in this trace



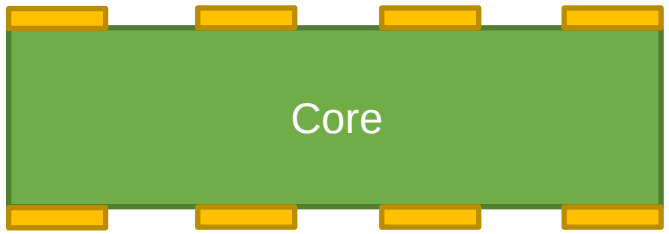
Much less skew in this weave style



What Not To Do

- 2-layer stackups are bad for high speed design:

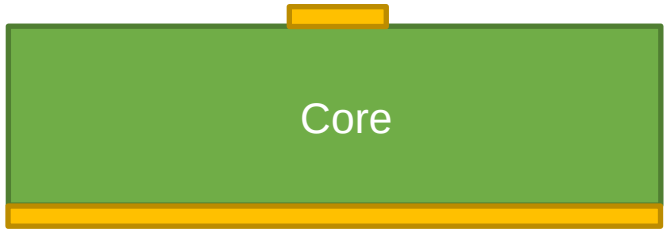
Worst



SIG

SIG

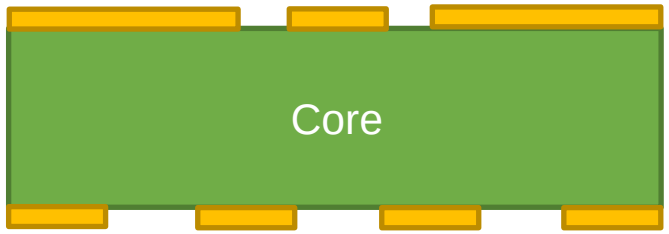
Less bad



SIG

GND

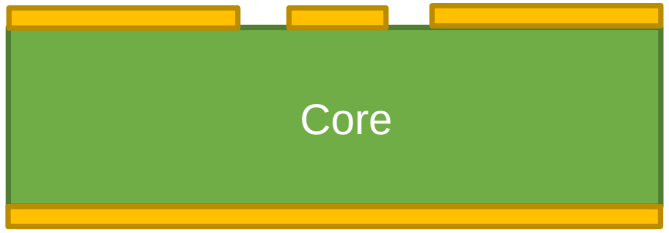
Less bad



SIG/GND

SIG

Okay



SIG/GND

GND

Start With 4 or More Layers

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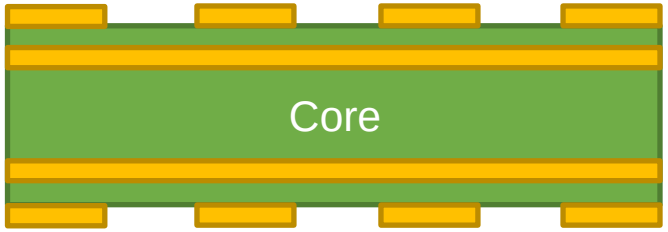
- 4-layer stackups are the starting point for high speed PCBs:

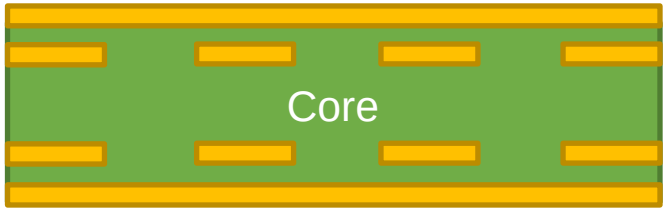
Acceptable



High speed SIG + routed PWR
GND

PWR
Low speed SIG, other components

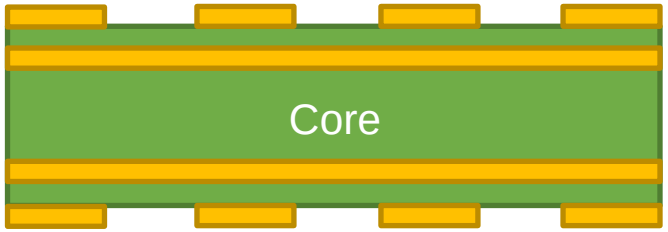
Better



GND
High speed SIG + routed PWR

High speed SIG + routed PWR
GND

Best



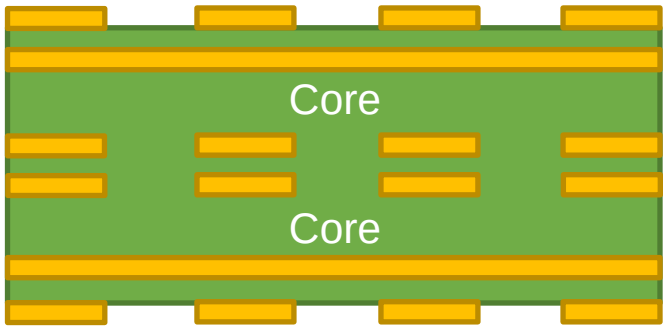
High speed SIG + routed PWR
GND

GND
High speed SIG + routed PWR

Start With 4 or More Layers

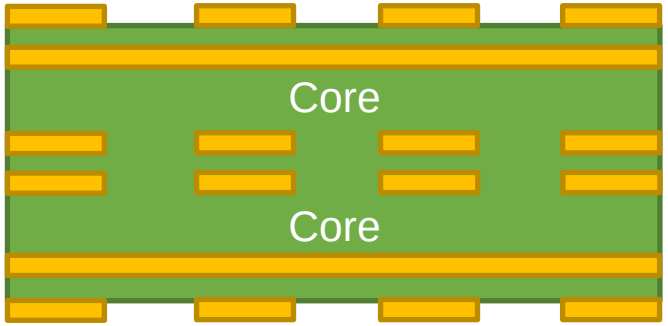
- Use a 6-layer stackup for higher power demands at high speed

Not Preferred:

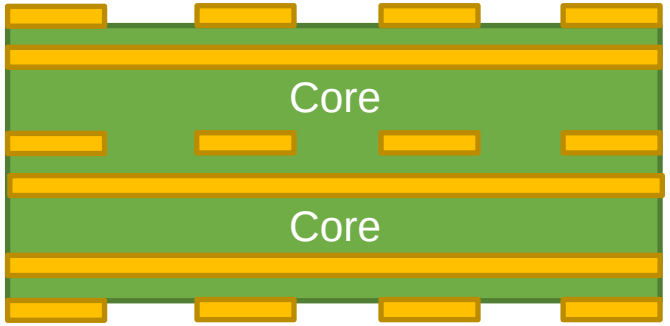


High speed SIG
GND
SIG
SIG
PWR
High speed SIG

Preferred:



SIG + PWR
GND
PWR
SIG
GND
SIG + PWR

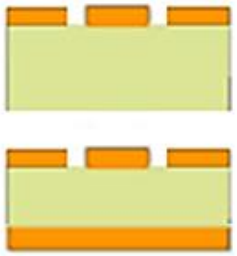


SIG + PWR
GND
PWR
GND
GND
SIG + PWR

Impedance and Routing

Impedance and Propagation

$$Z_0 = \sqrt{\frac{R+i\omega L}{G+i\omega C}},\quad \gamma = \sqrt{(R+i\omega L)(G+i\omega C)} \rightarrow v = \frac{1}{\sqrt{LC}} \text{ (lossless)}$$



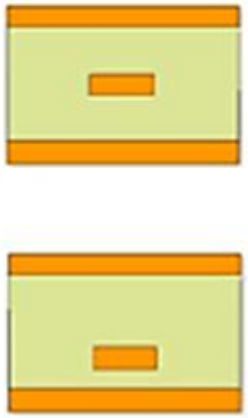
Coplanar microstrip $v = \frac{c}{\sqrt{Dk_{eff}}}$

Coplanar microstrip w/ ground

- Lower losses, copper pour allows for thinner 50 Ohm traces

Microstrip $v = \frac{c}{\sqrt{Dk_{eff}}}$

- Lower losses, wider traces



Symmetric stripline

$v = \frac{c}{\sqrt{Dk}}$

Asymmetric stripline

- Higher losses, but traces can be much thinner than on the surface layer

Microstrip Impedance

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- IPC-2141: $$Z_0 = \frac{87}{(\varepsilon_r + 1.41)^{0.5}} \ln\left(\frac{5.98h}{0.8w + t}\right)$$ **(Only accurate for 50 Ohm traces)**

- Wadell's Equations: **(Highly accurate)**

$$Z_0 = \frac{60}{(2\varepsilon_r + 2)^{0.5}} \ln\left(1 + \frac{4h}{w'}\left[\left(\frac{14 + \frac{8}{\varepsilon_r}}{11}\right)\left(\frac{4h}{w'}\right) + \sqrt{\left(\frac{14 + \frac{8}{\varepsilon_r}}{11}\right)^2 \left(\frac{4h}{w'}\right)^2 + \pi^2 \frac{1 + \frac{1}{\varepsilon_r}}{2}}\right]\right)$$

where $$w' = w + \left(\frac{1 + \frac{1}{\varepsilon_r}}{2}\right)\left(\frac{t}{\pi}\right) \ln\left(\frac{4e}{\left(\frac{t}{h}\right)^2 + \left(\frac{1/\pi}{w/t + 1.1}\right)^2}\right)$$

and $$\varepsilon_{eff} = \begin{cases} \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(\left(1 + \frac{12h}{w}\right)^{-0.5} + 0.04\left(1 - \frac{w}{h}\right)^2\right) & \text{if } w < h \\ \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + \frac{12h}{w}\right)^{-0.5} & \text{if } w > h \end{cases}$$

Stripline Impedance

Altium

- IPC-2141:

$$Z_0 = \frac{94.15}{\sqrt{\varepsilon_r}\left(\frac{W}{B-T} + \frac{C_f}{\pi}\right)} \quad \text{when } \frac{W}{B} > 0.35$$

(Only accurate for 50 Ohm traces)

$$\text{where } C_f = \frac{2B}{B-T}\left(\ln\left(\frac{B}{B-T}+1\right) - \left(\frac{T}{B-T}\right)\ln\left(\frac{1}{(1-T/B)^2}-1\right)\right)$$

- Wadell's Equations:

(Highly accurate)

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} ln\left[1 + \frac{8h}{\pi W_{eff}}\left(\left(\frac{16h}{\pi W_{eff}}\right) + \sqrt{\left(\frac{16h}{\pi W_{eff}}\right)^2 + 6.27}\right)\right]$$

$$\text{where} \quad W_{eff} = W + \frac{T}{\pi} ln\left[\frac{\varepsilon_r}{\sqrt{\left(\frac{T}{4H+T}\right)^2 + \left(\frac{\pi T}{4(W+1.1T)}\right)^m}}\right] \quad \text{and} \quad m = \frac{6H}{3H+T}$$

$$\text{when } \frac{W}{B} < 0.35,\ \frac{T}{B} < 0.25, \text{ or } \frac{T}{W} < 0.11$$

- Comparison of impedance determination methods

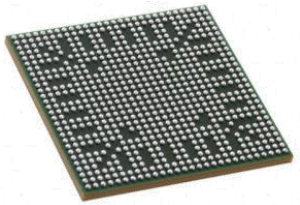
Method	Accuracy	Difficulty	Time
IPC-2141	Lowest	Lowest	Lowest
Wadell's Equations	Moderate	Moderate	Moderate to High
2D Field Solver, No Losses	High	Low	Low
2D Field Solver With Losses	High	Low	Moderate
3D Field Solver	Highest	Highest	Highest

- Altium Designer includes a 2D field solver

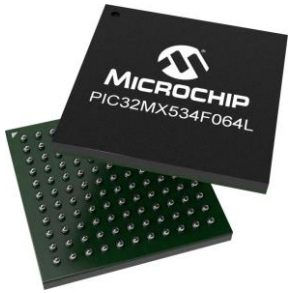
Ball Grid Arrays (BGAs)

- Many high-speed processors come in BGA packages
  - FPGAs
  - MCUs/MPUs
  - SoCs and ASICs
  - Application processors
- Need to design stackup to support routing

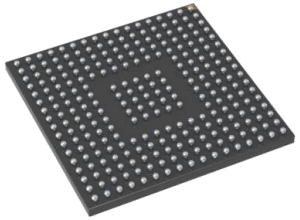
AM387x Sitara (684 pins, PCIe, HDMI, LVDS, DDR2)



PIC32 (121 pins, USB, Ethernet)



STM32 (176 pins, USB, HDMI, Ethernet, DDR2)

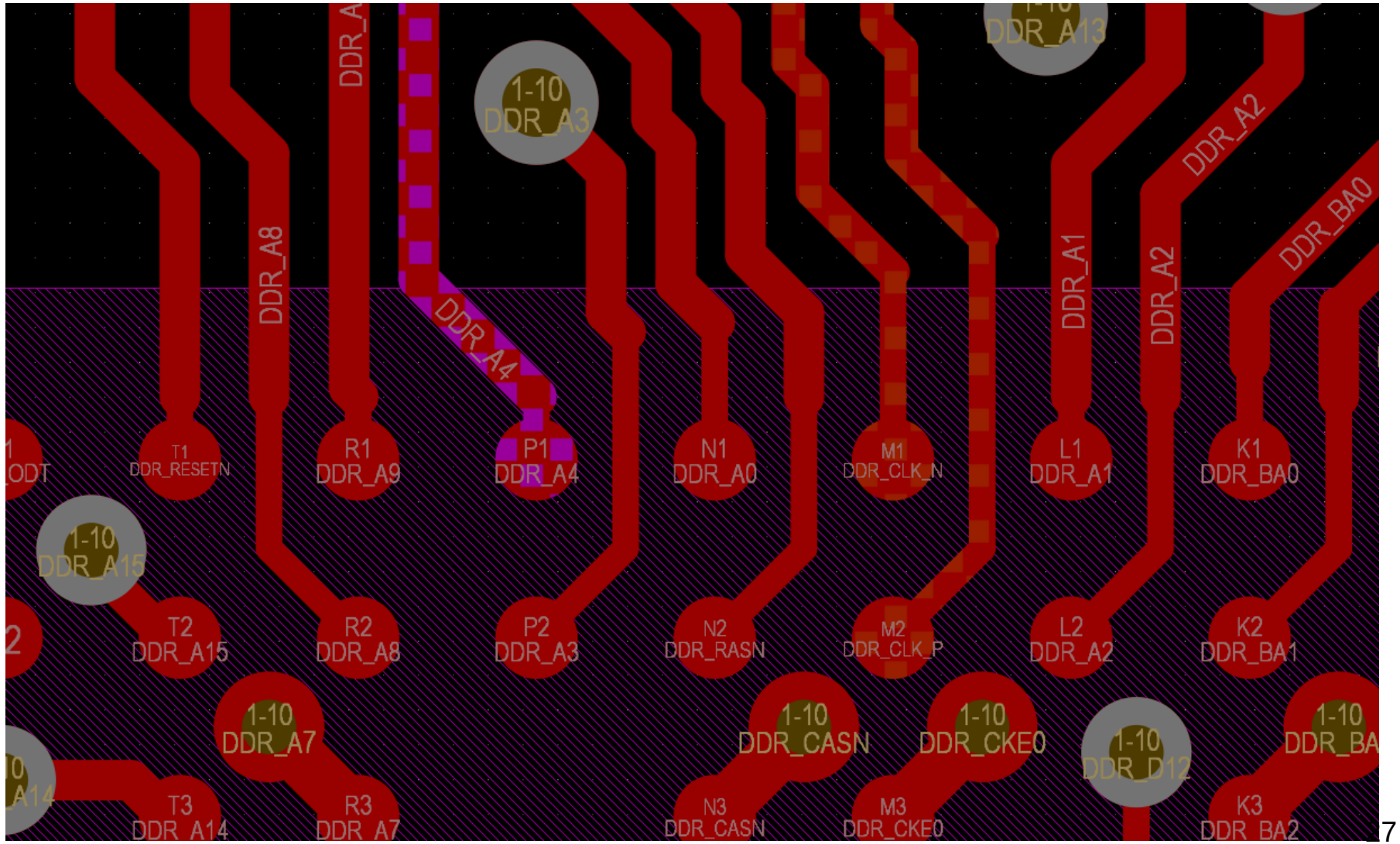


Xilinx FPGA (High pin count, all of the above)

Trace Width and Spacing Calculation

Altium

- Neck-down routing into the BGA
- Used on single-ended and differential clock
- Okay for lower speed (10/100 Ethernet, Low-speed USB, etc.)

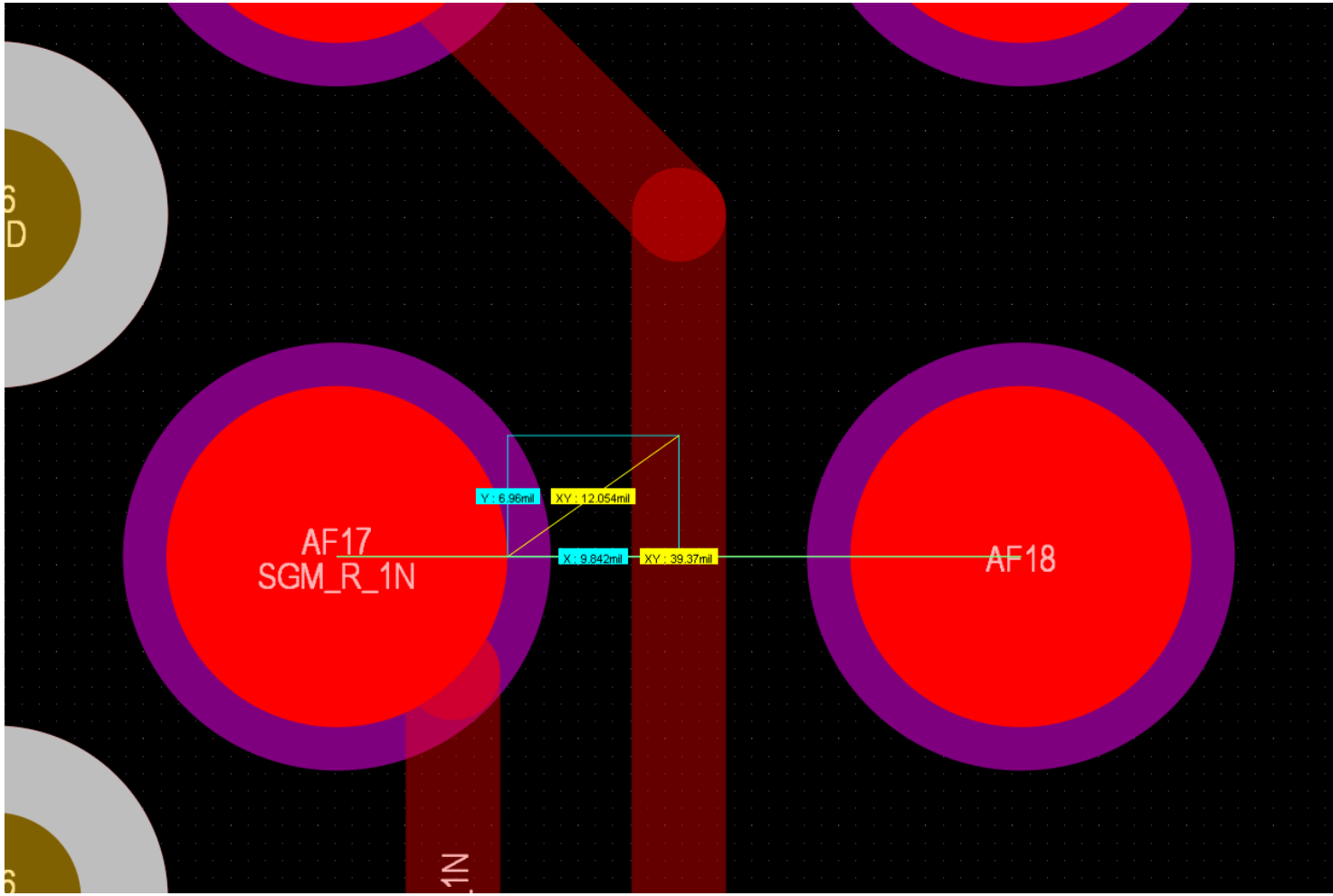


Trace Width and Spacing Calculation

- 1 mm pitch, large pad size (0.5 mm diameter)

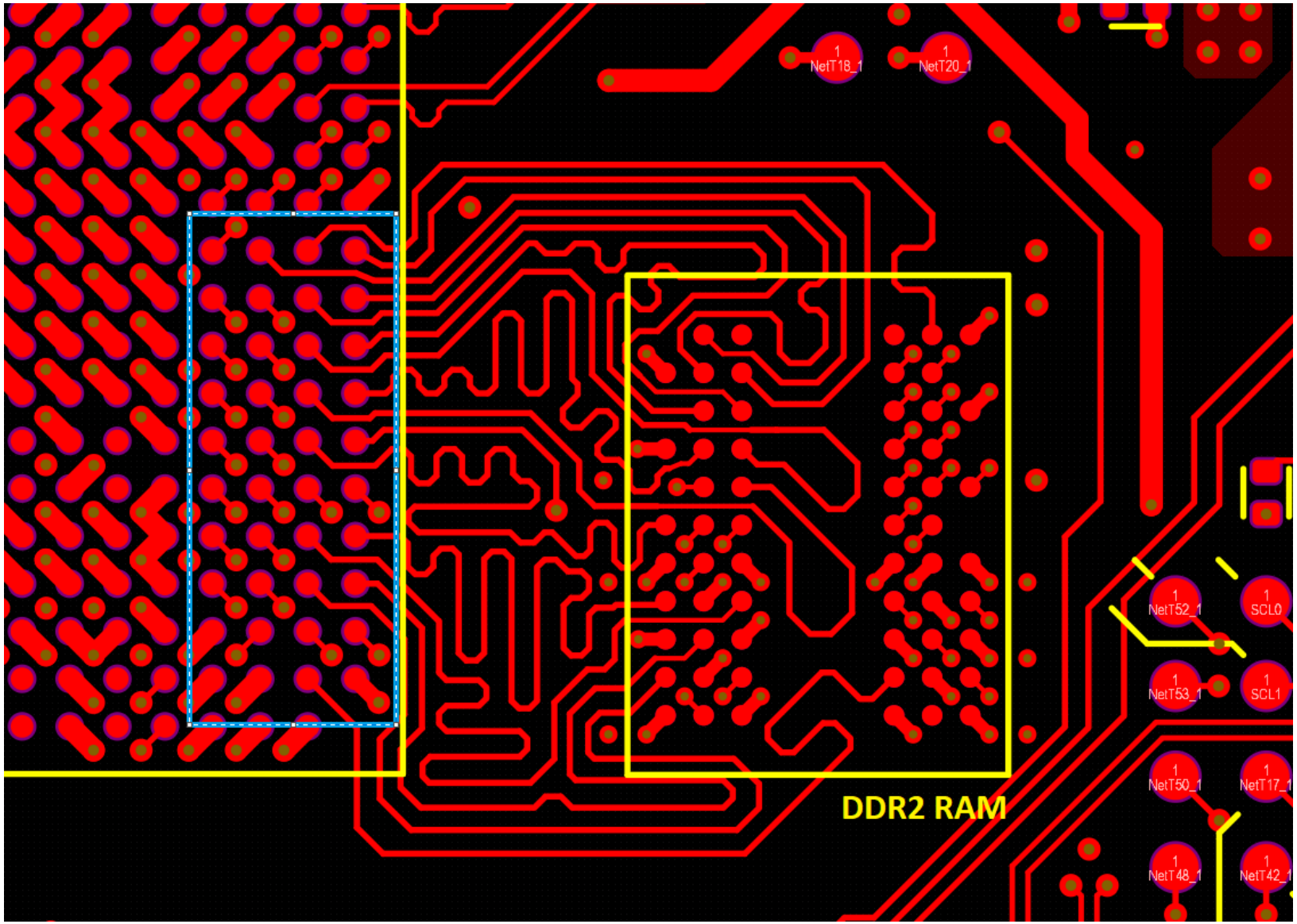
- 5 mil feature clearance → 9.684 mil maximum trace width

- Use this and layer thickness to determine spacing



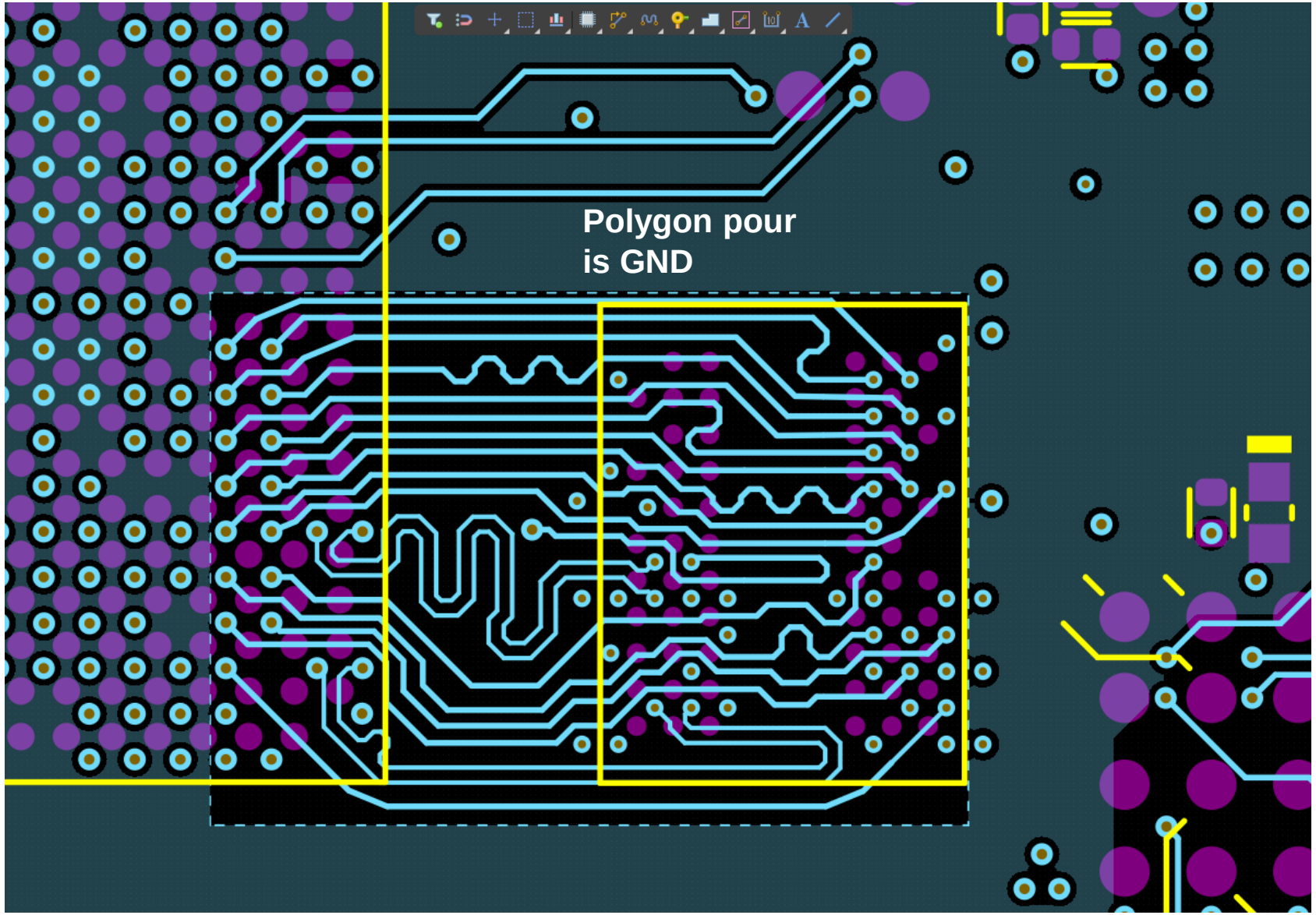
Routing Example (Single DDR2 Chip)

- Layer 1 on 6-layer board
- DDR2 routing spread across 2 layers
- Length matching sections are visible



Routing Example (Single DDR2 Chip)

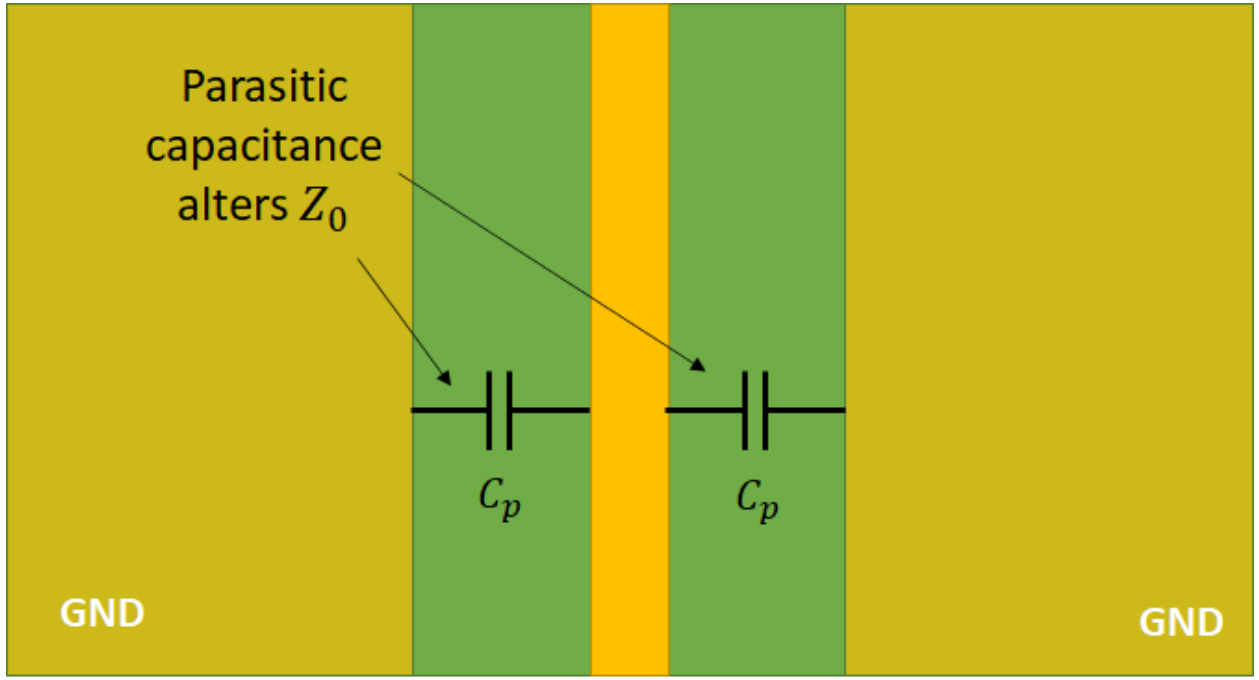
- Layer 4 on same 6-layer board
- DDR2 routing with striplines
- Notice the cutout in the GND polygon
- L2 and L5 are GND
- L3 is PWR



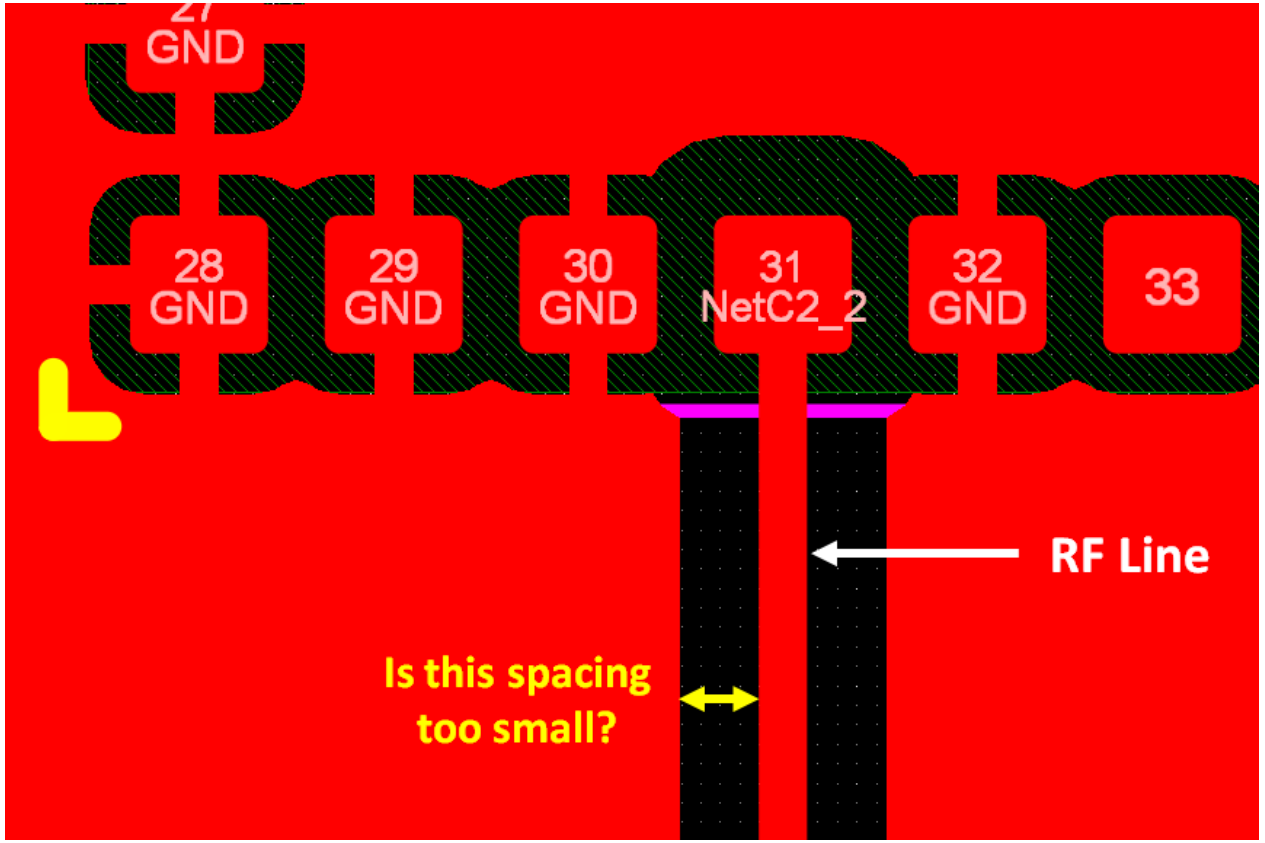
Routing Example – Why the cutout?

Altium

- What's the allowed pour clearance near controlled impedance traces?



$$Z_0 = \sqrt{\frac{L}{C_{total}}} = \sqrt{\frac{L}{C + 2C_p}}$$



Myths and Misconceptions

- **All of these statements are wrong or taken out of context**
  - Ferrites are the only way to isolate power rails
  - Backdrill all stubs if routing through vias
  - Filling with copper pour is always good/bad
  - All high-speed boards need low-Dk/PTFE laminates
  - Differential pairs must always be routed very close to each other
  - Right-angle traces make high speed boards fail EMI tests

Thank You!

Stay tuned for our Altium Designer demonstration.